## In the claims:

1	1.	( Previously Amended) A computer system comprising:
2		a processor including:
3		a central processing unit (CPU) core to execute non-graphic instructions;
4		a graphics core to compute graphical transformations via supersampling
5		techniques; and
6		a unified graphics cache coupled to the graphics core, wherein the unified
7		graphics cache stores texture data, color data and depth data.
1	2.	(Unchanged) The computer system of claim 1 wherein the graphics cache
2		comprises:
3		a texture cache to store texture data; and
4		a color and depth buffer to store the color data and the depth data.
1	3.	(Previously Amended) The computer system of claim 1 further comprising:
2		a CPU cache coupled to the CPU core.
1	4.	(Unchanged) The computer system of claim 3 further comprising a bus interface
2		coupled to the CPU cache and the graphics cache.
1	5.	(Previously Amended) The computer system of claim 1 wherein the
2		graphics core performs rendering according to a tile-based rendering architecture.
1	6.	(Previously Amended) The computer system of claim 1 further comprising:
2		a bus interface coupled to CPU cache and the graphics cache; and
3		a main memory coupled to the bus interface.

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- 1 7. (Unchanged) The computer system of claim 2 wherein the graphics core
- 2 amplifies image polygons and renders the polygons into the graphics cache.
- 1 8. (Previously Amended) The computer system of claim 7 wherein
- 2 amplification of the image polygons are implemented via viewport transformation.
- 1 9. (Unchanged) The computer system of claim 7 wherein the graphics core
- 2 downsamples the image polygons after the polygons have been rendered.
- 1 10. (Unchanged) The computer system of claim 9 wherein the downsampling of the
- 2 image polygons are implemented by executing a bit aligned block transfer.
- 1 11. (Previously Amended) A method for supersampling an image comprising:
- 2 receiving polygons of a first tile of the image at a graphics core; and
- amplifying the polygons at the graphics core;
- 4 rendering the polygons of the first tile into a unified graphics cache, wherein the
- 5 unified graphics cache stores texture data, color data and depth data of the image.
- 1 12. (Previously Amended) The method of claim 11 further comprising
- 2 executing a stretch aligned block transfer at the graphics core after rendering the
- 3 polygons.
- 1 13. (Previously Amended) The method of claim 11 wherein the polygons are
- 2 amplified four times the original size of the image.
- 1 14. (Previously Amended) The method of claim 11 wherein the amplification
- 2 is achieved using viewport transformation.

- 1 15. (Unchanged) The method of claim 11 wherein the process of rendering the
- 2 polygons comprises:
  - setting up the image polygons; and rasterizing pixels within the image polygons.
- 1 16. (Unchanged) The method of claim 15 further comprising texturing the pixels
- 2 within the image polygons.
- 1 17. (Unchanged) The method of claim 11 further comprising downsampling the
- 2 polygons after the polygons have been rendered.
- 1 18. (Unchanged) The method of claim 17 wherein the downsampling is achieved by
- 2 executing a bit aligned block transfer.
- 1 19. (Unchanged) The method of claim 11 further comprising:
- determining whether the unified graphics cache includes more tiles that are to be
- 3 rendered; and
- if so, receiving polygons of a second tile of the image at the graphics core; and
- 5 rendering the polygons of the second tile into the unified graphics cache.
- 1 20. (Previously Amended) A central processing unit (CPU) comprising:
- 2 a CPU core to execute non-graphic instructions;
- 3 CPU cache coupled to the CPU core;
- a graphics accelerator to compute graphical transformations via supersampling
- 5 techniques; and

- 6 a unified graphics cache coupled to the graphics core and the CPU, to store
- 7 texture data, color data and depth data.
- 21. (Unchanged) The CPU of claim 20 wherein the graphics cache comprises:
- 2 a texture cache to store texture data; and
- a color and depth buffer to store the color data and the depth data.

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- 22. 2 (Previously Amended) The CPU of claim 20 wherein the graphics core
- amplifies image polygons and renders the polygons into the graphics cache. 3
- 23. 1 (Unchanged) The CPU of claim 22 further comprising a bus interface coupled to
- the CPU cache and the graphics cache. 2
- 24. (Previously Amended) The CPU of claim 23 wherein the graphics
- accelerator performs rendering according to a tile-based rendering architecture. 2

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